SoC Centric

Production-ready embedded Linux for *AMD Xilinx Zynq*

A custom Yocto/PetaLinux-based platform for Zynq-7000, UltraScale+ MPSoC, Versal, and Kria SOMs — processing system and programmable logic, engineered as one platform.

Validated on **Zynq-7000** · **UltraScale+ MPSoC** · **Versal AI Edge** · **Kria KV260/KR260**

Real-time on the Cortex-R5F RPU (FreeRTOS / Zephyr, OpenAMP)

Request an evaluation image →

THE PLATFORM

Processing system and programmable logic — engineered as one platform.

PetaLinux and ad-hoc bitstream handling get you running — but PS, PL, and the real-time domain rarely ship as one versioned, reproducible whole.

One versioned build unifies the boot chain, kernel, rootfs, FPGA bitstream, and the real-time RPU domain — reproducible and owned by you.

Our Zynq platform is a reproducible, Yocto-built platform for the AMD adaptive-SoC portfolio. It unifies the full boot chain (FSBL/PMU firmware, ATF, U-Boot), kernel, rootfs, FPGA bitstream management, and the real-time RPU into a single versioned build — so the processing system and programmable logic ship and update together.

VALIDATED HARDWARE

Zynq-7000 · UltraScale+ MPSoC · Versal AI Edge · Kria KV260 / KR260 — PS and PL unified in one reproducible, customer-owned build.

8 yrs
building production embedded Linux platforms

6
SoC platform families — ~90% of the embedded Linux market

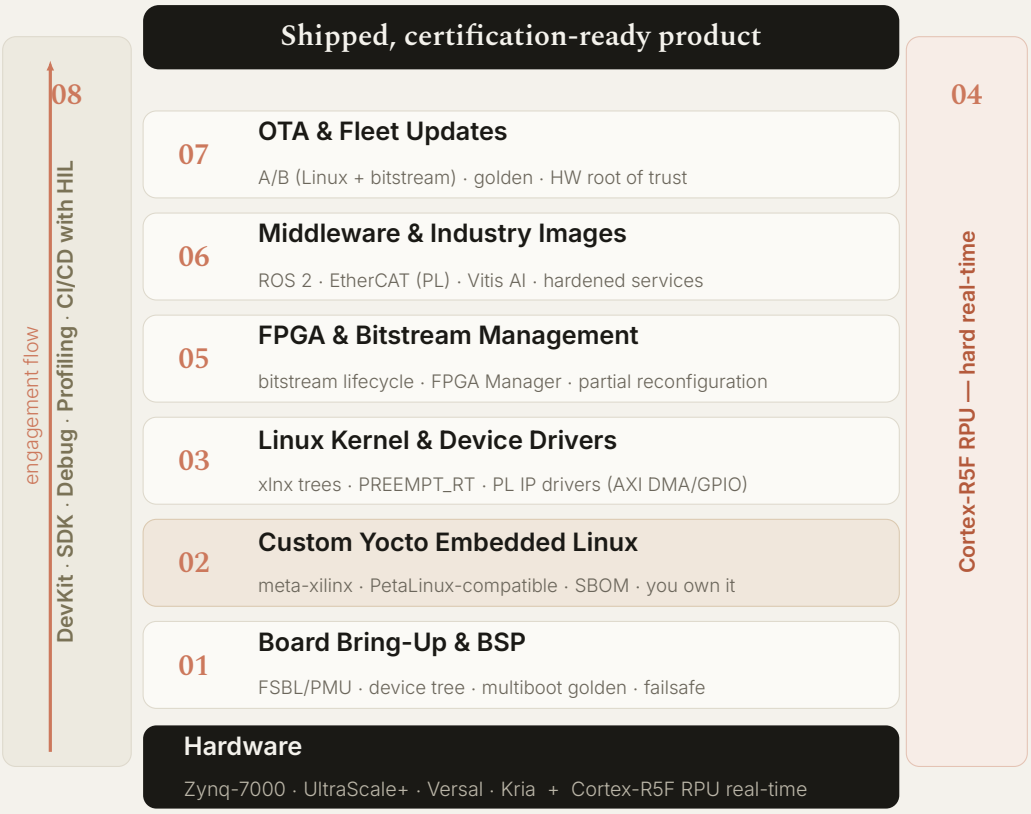
1
engineering methodology, applied across every platform

[Add your proof point here] e.g. "Delivered a unified PS+PL Zynq platform for an industrial customer — atomic Linux-plus-bitstream OTA, zero field bricks." One concrete, anonymized outcome here will do more for credibility than any claim on the following pages. Replace this box before sending.

HOW IT FITS TOGETHER

The platform stack

Hardware comes alive at the bottom and ships as a maintainable product at the top. Developer tooling spans the whole engagement; the real-time domain runs the hard-real-time path alongside Linux.



Each layer is a capability detailed on the following pages.

Hardware & product · Owned OS foundation · Real-time domain · Spans the engagement

01 CAPABILITY

Board Bring-Up & BSP

> *Your Zynq board boots reliably — processing system and programmable logic, brought up together.*

The foundation layer: a clean boot chain across the PS, with the PL configured and verified as part of bring-up.

- **Schematic / pin review** — MIO/EMIO planning, DDR config, and power sequencing.
- **Custom FSBL & PMU firmware** — configured for your board.
- **Device tree for PS & PL** — peripherals and PL IP, with overlays per bitstream.
- **Bring-up & smoke test** — memory calibration, peripheral checkout, PL config check.
- **Custom bootloader** — U-Boot board port, boot.scr logic, QSPI/eMMC/SD strategy.
- **Golden boot & failsafe** — QSPI fallback with multiboot register support, watchdog rollback.

TECHNICAL DETAIL

Boot chain	**BootROM→FSBL→ATF→U-Boot**	Recovery	**Multiboot golden**
Storage	**QSPI / eMMC / SD**	PL	**Per-bitstream DT**

You receive: custom FSBL/PMU config, device tree with PL overlays, a bring-up report, bootloader, and golden-boot setup.

02 CAPABILITY

Custom Yocto Embedded Linux

> *One reproducible build for Linux, RPU firmware, and bitstream — owned by you.*

Replacing ad-hoc PetaLinux flows with a reproducible build that versions the whole stack together.

- **Reproducible builds** — meta-xilinx, PetaLinux-compatible, Yocto rel-v2025.x.
- **PS + PL as one image** — Linux, RPU firmware, and bitstream versioned together.
- **Minimal & locked down** — read-only rootfs, hardened services.
- **You own everything** — full source, build system, recipes.
- **Auditable & maintainable** — SBOM, CVE patching, mainline alignment.
- **Manufacturable** — one reproducible build flashed identically.

TECHNICAL DETAIL

Build system	**Yocto / BitBake**	BSP layer	**meta-xilinx**
Compatibility	**PetaLinux**	Supply chain	**SBOM + signed**

You receive: a full source tree & build system that versions Linux, RPU firmware, and bitstream together, plus an SBOM and docs.

03 CAPABILITY

Linux Kernel & Device Drivers

> *A hardened Zynq kernel with first-class drivers for your custom PL IP.*

Shaping the kernel to your design — including drivers for the programmable-logic IP that makes Zynq unique.

- **Kernel customization** — xlnx trees, hardening, mainline alignment.
- **PREEMPT_RT** — porting and latency validation.
- **Boot streamlining** — FSBL-to-userspace budgets.
- **PL IP drivers** — AXI DMA, AXI GPIO, custom AXI peripherals (UIO or kernel drivers).
- **Camera & PS drivers** — V4L2 MIPI CSI & PL ISP; CAN, SPI, I2C, GEM Ethernet, USB.

TECHNICAL DETAIL

Kernel	**xlnx trees**	Real-time	**PREEMPT_RT**
PL drivers	**AXI DMA / GPIO**	Camera	**V4L2 CSI / PL ISP**

You receive: a tuned kernel config, PL IP drivers (UIO or kernel), PS peripheral drivers, and RT validation.

04 CAPABILITY

Real-Time Domain (Cortex-R5F RPU)

Hard real-time on the RPU, coordinated with Linux over OpenAMP.

The UltraScale+ RPU runs hard real-time alongside the Linux APU, coordinated over OpenAMP — for motion control and safety.

- **FreeRTOS & Zephyr on the RPU** — lockstep or split Cortex-R5F.
- **OpenAMP / RPMsg** — between Linux (APU) and RTOS (RPU).
- **Deterministic control** — motor control, safety supervision, deterministic I/O on the RPU.
- **Mixed-criticality** — partitioning across PS, PL, and RPU.

TECHNICAL DETAIL

RT core	**Cortex-R5F RPU**	RTOS	**FreeRTOS / Zephyr**
Comms	**OpenAMP / RPMsg**	Mode	**lockstep or split**

You receive: RPU firmware, the OpenAMP/RPMsg link, and a documented mixed-criticality partition across PS, PL, and RPU.

05 CAPABILITY

FPGA & Bitstream Management

> *Programmable logic managed as a first-class, versioned, signable part of the platform.*

Zynq's defining strength is programmable logic. We treat the bitstream as a first-class platform artifact — versioned, signed, and updatable alongside Linux.

- **Bitstream lifecycle** — versioning, signing, and packaging into the platform build.
- **Runtime loading** — via FPGA Manager, with device tree overlays per design.
- **Partial reconfiguration** — live PL updates without a full reload.
- **PL IP integration** — AXI register maps, interrupt wiring, DMA design.
- **PL driver development** — UIO / kernel modules and userspace APIs.
- **PS/PL co-validation** — interface stress and timing verification.

TECHNICAL DETAIL

Loading	**FPGA Manager**	Update	**Partial reconfig**
Integration	**AXI / DMA / IRQ**	Drivers	**UIO / kernel**

You receive: a versioned, signed bitstream pipeline, PL drivers and userspace APIs, and PS/PL co-validation.

06 CAPABILITY

Middleware & Industry Images

> *Ship faster with a hardened, PL-accelerated image instead of a blank build.*

Pre-integrated platform variants tuned per industry — the right stack, with PL acceleration where it counts, on day one.

Robotics
ROS 2 on KR260, PL-accelerated perception, time-synced I/O.

Industrial
Modbus, OPC UA, EtherCAT (PL-assisted), TSN.

Automotive
SocketCAN, RT patch, gateway architectures.

Vision & DSP
GStreamer with PL acceleration, Vitis AI runtime.

Medical
traceable builds, SBOM, IEC 62304-aligned workflow.

Defense / Aerospace
hardened, audit-ready, DO-178C-aligned.

Also available: high-speed acquisition, SDR, and custom-protocol variants — or a variant built to your vertical.

PRODUCTION BASELINE — EVERY VARIANT

Filesystem	**Read-only + overlayfs**	Resilience	**Watchdog recovery**
Services	**Hardened daemons**	Tamper / power loss	**Survives both**

You receive: an industry image pre-integrated with the relevant stack and PL acceleration, hardened to the production baseline.

07 CAPABILITY

OTA & Fleet Updates

Update Linux and bitstream together, atomically, across the fleet.

On Zynq, an update is more than an OS image — the programmable logic updates with it, atomically, with a guaranteed way back.

- **Full-stack A/B** — aware of both Linux images and FPGA bitstreams — atomic update.
- **Golden recovery** — golden image plus golden bitstream.
- **Auto rollback** — health-checked, automatic.
- **Fleet management** — cloud or on-prem, staged rollouts, delta updates.
- **Dashboard** — upload, target, monitor, one-click rollback.
- **Signed & secure** — chained to the hardware root of trust.

TECHNICAL DETAIL

Scope	**Linux + bitstream**	Scheme	**A/B + golden**
Rollout	**Staged + delta**	Trust	**HW root of trust**

You receive: a full-stack OTA pipeline updating Linux and bitstream atomically, the server, the dashboard, and signed updates.

08 CAPABILITY

DevKit, SDK, Debug & Profiling

> *Your team owns and operates the platform — PS and PL — no black box.*

Spans the whole engagement: tooling for your own team to develop, debug, and rebuild both the software and the logic.

- **Evaluation images** — for Kria KV260/KR260 and ZCU boards.
- **Application SDK & Yocto eSDK** — cross-toolchain plus the full build workflow.
- **Cross-debug** — JTAG via Vivado hardware manager, kgdb, gdbserver.
- **Profiling & CI/CD** — perf, LTTng, PL/PS utilization; image+bitstream builds with HIL.

TECHNICAL DETAIL

Eval	**Kria / ZCU**	SDKs	**App + eSDK**
Debug	**Vivado JTAG / kgdb**	Pipeline	**image+bitstream CI**

You receive: eval images, both SDKs, Vivado/JTAG debug setup, and a CI/CD pipeline building image and bitstream with HIL.

WHY US

Why SoC Centric

One engineering methodology, applied with the rigor of a regulated-industry supplier.

- Replaces ad-hoc vendor images with a reproducible, owned, manufacturable platform built to ship.
- You own everything — full source, build system, and documentation. No lock-in, to us or anyone.
- Reproducible Yocto builds with SBOMs — **certification-ready** for ISO 26262, IEC 62304, IEC 61508, and DO-178C environments.
- The only platform here with programmable logic — PS and PL delivered, versioned, and updated as one.
- Part of a platform family covering ~90% of the embedded Linux market, with one consistent methodology.
- A natural growth path: platform → independent verification & validation → hardware-in-the-loop testing → field data logging.

GETTING STARTED

How an engagement begins

01
Eval image
We send a working platform image for your board to evaluate — no commitment.

02
Architecture call
A 30-minute call to map your hardware, industry, and target to a plan.

03
Pilot
A scoped bring-up + Yocto build on your actual board, with deliverables.

04
Platform delivery
Full source, build system, OTA, and tooling — handed over, owned by you.

GET STARTED

Let's talk

Ready to turn your Zynq project into a product?

PetaLinux gets you running. We turn Zynq into a product where the processing system and programmable logic ship, certify, and update as one.

→ Request an evaluation image for your board | → Schedule a 30-minute platform architecture call

GET IN TOUCH

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SOC CENTRIC

Production embedded Linux platforms across NVIDIA Jetson · AMD Xilinx Zynq · NXP i.MX · TI Sitara · Intel/AMD x86 · Raspberry Pi.

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